REMARKS

Claims 1-7 are all the claims pending in the application.

Claim 1 is rejected under 35 U.S.C. § 102(b) as being anticipated by Strole et al.

Claims 2-7 are objected to as being dependent upon a rejected base claim.

The Applicants traverse the rejections and request reconsideration.

The Examiner contends that in Section V of Strole consideration of hardware overheads is disclosed. The Applicants respectfully submit that the Examiner is mischaracterizing the teachings of Strole. In our analysis, there is no teaching in Section V of Strole (or anywhere else) regarding hardware overheads being considered as required by the present invention.

In Strole's scheme, the test pattern generator is implemented in a separate chip, called TESTCHIP, which comprises a RAM to store weight information, an LFSR, weight generation logic, and counters. This scheme is not a built-in self-test unlike embodiments of the present invention, as recited in claim 1.

Since it is not practical to redesign a new TESTCHIP for every different circuit under test, hardware of the TESTCHIP is fixed and independent of the circuit under test in Strole. In such a scheme, optimizing hardware overhead is believed to be meaningless. In fact, Strohe does not mention hardware overhead at all because, as discussed above, there is no need for optimizing based on hardware overhead in Strole's scheme.

The optimization objective in Strole is merely to reduce weight set sizes such that all weight sets fit into the RAM. If weight sets are too big to fit into the RAM, a new weight set is loaded multiple times during test application resulting in longer test application time.

In contrast, an embodiment of the present invention is a built-in self-test where the test pattern generator resides with the circuit under test on the same chip. In such architecture, unlike

in Strohe, hardware overhead is dependent on the circuit under test. This is because, hardware of the test pattern generator is synthesized from the set of deterministic patterns for the circuit under test. In such a built-in self-test architecture, the pattern generator is fully customized for the circuit under test. Since the test pattern generator is implemented on the chip, it is important to minimize hardware overhead. Therefore, the present invention, as recited in claim 1, **considers hardware overheads when each new testcube is added.**

As noted above, Strole has no need to consider hardware overheads in adding test patterns and does not disclose (or even remotely suggest) considering hardware overheads.

Claim 1 should be allowed at least because Strole does not disclose considering hardware overheads when each new testcube is added.

Claims 2-7 have been found allowable but for their dependence on a rejected base claim. The Examiner is requested to hold the status of these claims in abeyance pending resolution of the status of the base claim.

Applicants hereby petition for any extension of time which may be required to maintain the pendency of this case, and any required fee, except for the Issue Fee, for such extension is to be charged to Deposit Account No. 19-4880.

Respectfully submitted,

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